A 2-GHz Three-Stage AlInAs–GaInAs–InP HEMT MMIC Low-Noise Amplifier

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Abstract—**A three-stage monolithic microwave integrated circuit (MMIC) low-noise amplifier (LNA) has been fabricated using 0.15-μm gate-length InP-based (AlInAs–GaInAs) high electron mobility transistor (HEMT) technology. The LNA exhibited less than 0.5-dB noise figure and greater than 35-dB gain from 2.25 to 2.5 GHz. The input and output return loss exceeded 15 dB across the band. These results are believed to be the best reported to date from a MMIC amplifier in this frequency range.**

I. Introduction

THE PERFORMANCE of low-frequency microwave MMIC low-noise amplifiers is usually limited by the noise performance of the active devices (typically a GaAS MESFET or HEMT) and the losses of the input and output matching circuits. These factors make the simultaneous realization of an ultra low-noise figure, a high input and output return loss, and high gain difficult. In addition, at the lower microwave frequencies (< 8 GHz), the use of distributed matching elements is prohibited in monolithic circuits because of the large size they would require. The lumped element matching approach can lead to additional losses that can further compromise performance.

Because of these limitations, the use of an ultra-low-noise transistor technology is extremely attractive for the realization of low-noise monolithic amplifiers. The AlInAs–GaInAs on InP HEMT is an ideal candidate for such an application, because its outstanding millimeter-wave low-noise performance [1], [2] also results in excellent microwave low-noise performance. Such a device provides the added design margin required to realize ultra-low-noise microwave MMIC amplifiers.

This letter will summarize the design, fabrication, and measured performance of an ultra-low-noise AlInAs–GaInAs on InP HEMT MMIC amplifier.

II. Device Structure and Circuit Fabrication

The process sequence for the AlInAs–GaInAs HEMT MMIC is similar to that for discrete devices, which was described in [3]. All the patterned layers were defined photolithographically, except for the gate layer which was defined with electron-beam lithography. Ohmic contact metal areas were first defined by lifting off AuGe–Ni–Au metallurgy. Typical ohmic contact resistances were 0.17 Ω/mm and typical sheet resistances of 230 Ω/□ were obtained. Next, device isolation was achieved by implantation of boron ions. The resulting planar surface (as opposed to a mesa isolation technique) is crucial to obtaining a high yield in the electron beam lithography process. After alloying the ohmic contacts, the 0.15 μm long T-gates were defined using a PMMA-PMAA bilayer resist scheme.

Next, gate recess etching was performed to achieve a desired pinch-off voltage of approximately −0.4V. A Ti–Pt–Au gate was then defined by electron beam evaporation and lift-off. The process was completed by defining a Ti–Pt–Au overlay metallization by lift-off and interconnecting the individual source contacts by an air-bridged scheme using conventional gold plating techniques. The yield of these devices was optimized using a procedure outlined in [4], which allowed the device yield of the large periphery devices to be acceptable for high-volume MMIC applications.

The $Al_{.48}In_{.52}$ As–$Ga_{.47}In_{.53}As$ HEMT structures were grown by MBE on an InP substrates in a Riber 2300 system. The sheet charge density and mobility for the layers were approximately 2.8×10^{12} cm−2 and 10 000 cm^2/V-S, respectively [4].

III. Design

The design goal was a 2.275 GHz MMIC LNA with greater than 30-dB gain, less than 0.8-dB noise figure, and greater than 15-dB input and output return loss. 1400 μm × 0.15 μm devices were employed to ease the input impedance matching at the frequency of interest. HEMT noise parameters and scattering (S-) parameters were measured on-wafer with microwave probes using the Hewlett-Packard 8510C automatic vector network analyzer and ATN NP5-B noise parameter test system. A plot of the measured typical minimum noise figure $F_{\min}$ and associated gain Ga vs. frequency over the 2 to 18 GHz measurement range is shown in Fig. 1.

Spiral inductors were used in the sources of the HEMTs to provide a low-loss series feedback path for each device. This technique transforms the conjugate and low-noise matching impedances toward the same value, which results in a well matched input with no degradation in amplifier noise figure [5]. The series feedback reduces the available gain in each stage, which results in a need for a three-stage rather than a two-stage design.

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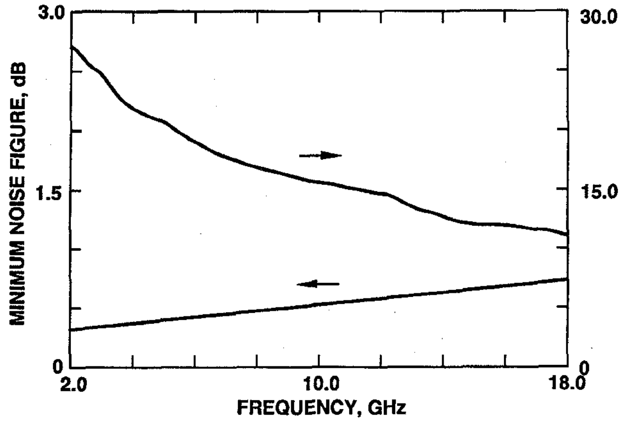

Fig. 1. Measured available gain and minimum noise figure for a 1400 μm $\times$ 0.15 μm AlInAs–GaInAs on InP HEMT.

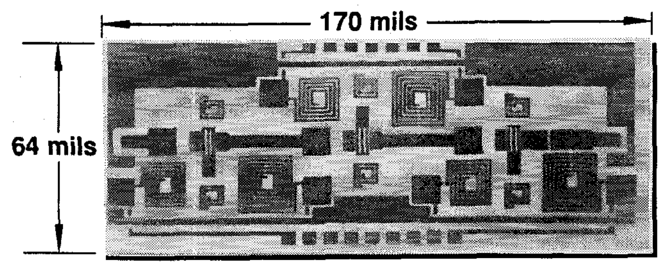

Fig. 2. Microphotograph of completed AlInAs–GaInAs on InP HEMT low-noise MMIC amplifier.

The design consists of three one-stage amplifiers in cascade to form the complete three-stage circuit. Lumped elements, including spiral inductors and metal-insulator-metal (MIM) capacitors, were used to synthesize the desired matching networks. The topology was chosen for maximum compaction. A microphotograph of the resulting circuit is shown in Fig. 2. The final die size was 4.3 mm by 1.6 mm.

IV. Experimental Results

The LNA gain and noise figure were measured on-wafer from 2.25 to 2.5 GHz. The noise-figure of the amplifier was less than or equal to 0.5 dB across the band; reaching a minimum of approximately 0.4 dB. The gain was greater than 35 dB below 2.475 GHz, and dropped slightly at 2.5 GHz. A plot of measured gain and noise figure is shown in Fig. 3. A plot of the measured input and output return loss is shown in Fig. 4. The response shows that the devices were well matched at both the input and output. The input return loss is approximately 14 dB across the band. The output return loss is approximately 20 dB across the band.

The performance of this circuit compares very favorably with previously reported MMIC low-noise amplifiers in this frequency range [6], [7], where the typical reported noise figures are in the 2.5 dB to 3.0 dB range.

V. Conclusion

We have designed and fabricated an AlInAs–GaInAs on InP 2.25-GHz HEMT MMIC LNA with greater than 35-dB gain and less than 0.5-dB noise figure. The input return loss

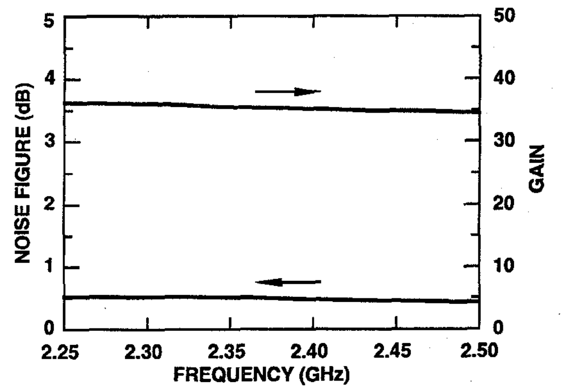

Fig. 3. Measured gain and noise figure of the InP HEMT low-noise MMIC amplifier.

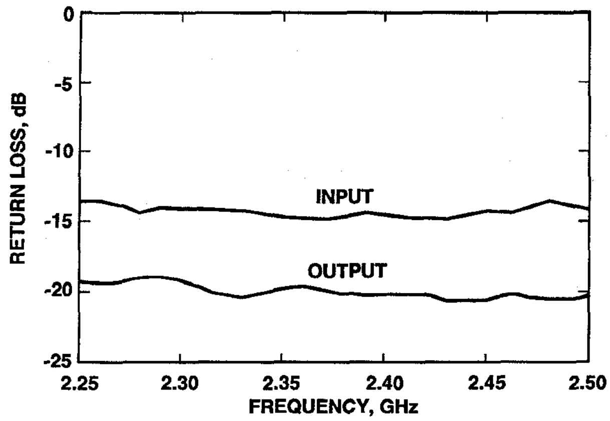

Fig. 4. Measured input and output return loss of the InP HEMT low-noise MMIC amplifier.

was approximately 14 dB and the output return loss was approximately 20 dB. This result demonstrates the outstanding low-noise potential of InP-based HEMT technology for the realization of low-noise MMIC amplifiers in the microwave frequency region.

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References

[1] L.D. Nguyen, L.E. Larson, and U.K. Mishra, "Ultra-high-speed modulation-doped field-effect transistors: A tutorial review," *Proc. IEEE*, vol. 80, no. 4, pp. 494–518, Apr. 1992.

[2] P.M. Smith and A.W. Swanson, "HEMT's—Low noise and power transistors for 1 to 100 GHz," *Appl. Microwave Mag.*, pp. 63–72, May 1989.

[3] U.K. Mishra, A.S. Brown, M.J. Delaney, P.T. Greiling, and C.F.

Krumm, "The AlInAs–GaInAs HEMT for microwave and millimeter-wave applications," *Trans. Microwave Theory Tech.*, vol. 37, pp. 381–387, Sept. 1989.
[4] L. Jelloian, L. Larson, S. Rosenbaum, A. Schmitz, M. Thompson, M. Lui, L. Nguyen, and U. Mishra, "Manufacturing study of yield and performance dependance on gate length for nanometer scale AlInAs–GaInAs HEMT's," *Dig. U.S. Conf. on GaAs Manufacturing Technol.*, Apr. 7–10, 1991, pp. 5–8.
[5] N. Ayaki, A. Inoue. T. Katoh, M. Komaru, M. Noda, and M. Kobiki, "A 12 GHz band monolithic HEMT low noise amplifier," in *Proc. Int. GaAs IC Symp.*, Nov. 1988, pp. 101–104.
[6] K. Chalapathi, B. Lakshmi, S. Jairam, and B. M. Arora, "Design of GaAs monolithic microwave amplifier low noise amplifier in L-band and SPST switch from DC to 2 GHz," *J. Inst. of Electron. Telecommun. Engineers*, vol. 36, no. 3–4, pp. 203–213, May–Aug. 1990.
[7] Y. Imai, M. Tokumitsu, A. Minakawa, "Design and performance of low-current GaAs MMIC's for L-band front-end applications," *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 2, pp. 209–215, Feb. 1991.